

## EAST Search History

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	154014	(martin.in. or langhammer.in.)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/02/13 12:44
L2	24	@ad<"20030911" and ((programmable adj logic adj device) or PLD) and L1 and ((logic adj array adj block\$1) or LAB\$2)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/02/13 12:44
L3	47	(martin.in. and langhammer.in.)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/02/13 12:44
L4	7	3 and ((programmable adj logic adj device) or PLD) and L1 and ((logic adj array adj block\$1) or LAB\$2)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/02/13 12:44
L5	2	("5027309"   "5493523").PN. OR ("6317771").URPN.	US-PGPUB; USPAT; USOCR	OR	ON	2007/02/13 12:51
L6	28277	("708"/\$.ccls. or "326"/\$.ccls.) and @ad<"20030911"	US-PGPUB; USPAT; USOCR	OR	ON	2007/02/13 12:52
L7	1288	6 and (logic adj array\$1) and (LUT\$1 or table\$1)	US-PGPUB; USPAT; USOCR	OR	ON	2007/02/13 12:53
L8	1141	7 and (programmable adj logic)	US-PGPUB; USPAT; USOCR	OR	ON	2007/02/13 12:54
L9	709	8 and rout\$3	US-PGPUB; USPAT; USOCR	OR	ON	2007/02/13 12:55
L10	299	(logic adj cell\$1) and 9	US-PGPUB; USPAT; USOCR	OR	ON	2007/02/13 12:56
L11	94	10 and (LAB or (logic adj array\$1 adj block\$1))	US-PGPUB; USPAT; USOCR	OR	ON	2007/02/13 12:57

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L12	21	11 and carry and sum	US-PGPUB; USPAT; USOCR	OR	ON	2007/02/13 13:03
L13	41	"708"/\$.ccls. and @ad<"20030911" and (LAB or (logic adj array\$1 adj block\$1)) and sum and carry	US-PGPUB; USPAT; USOCR	OR	ON	2007/02/13 13:07
L14	30	13 and (LUT\$1 or table\$1)	US-PGPUB; USPAT; USOCR	OR	ON	2007/02/13 13:08
S1	2	"5995991".pn.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/10/05 13:41
S2	2	"5065352".pn.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/10/04 15:20
S3	0	708/606.pn.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/10/04 15:21
S4	94	708/606.ccls.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/10/04 15:21
S5	20302	"708"/\$.ccls. and @ad<"20030911"	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/10/05 14:31
S6	648	S5 and (logic adj array\$1)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/10/05 13:42

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S7	460	S6 and (lut\$1 or table\$1)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/10/05 13:42
S8	425	S7 and (adder\$1 or adding or addition)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/10/05 13:43
S9	34	S8 and 708/700-714.ccls.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/10/05 13:43
S10	36	("4706216"   "5233539"   "5260610"   "5260611"   "5274581"   "5295090"   "5311080"   "5349250"   "5359242"   "5436574"   "5457644"   "5481206"   "5483478"   "5523963"   "5546018").PN. OR ("5761099").URPN.	US-PGPUB; USPAT; USOCR	OR	ON	2006/10/05 13:48
S11	244878	((programmable adj logic adj device) or PLD) and @ad<"20030911" nad ((logic adj array adj block\$1) or LAB\$2) and (LUT\$1 or table\$1)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/10/05 15:08
S12	1499	((programmable adj logic adj device) or PLD) and @ad<"20030911" and ((logic adj array adj block\$1) or LAB\$2) and (LUT\$1 or table\$1)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/10/05 14:56
S13	310	compress\$5 and S12	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/10/05 14:34
S14	148784	(martin.in. or langhammer.in.)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/10/05 14:34

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S15	1	S13 and S14	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/10/05 14:35
S16	18	((programmable adj logic adj device) or PLD) and S14 and ((logic adj array adj block\$1) or LAB\$2) and (LUT\$1 or table\$1)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/10/05 14:56
S17	1	S12 and 708/700-714.ccls.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/10/05 14:56
S18	36	("4706216"   "5233539"   "5260610"   "5260611"   "5274581"   "5295090"   "5311080"   "5349250"   "5359242"   "5436574"   "5457644"   "5481206"   "5483478"   "5523963"   "5546018").PN. OR ("5761099").URPN.	US-PGPUB; USPAT; USOCR	OR	ON	2006/10/05 14:57
S19	36	("4706216"   "5233539"   "5260610"   "5260611"   "5274581"   "5295090"   "5311080"   "5349250"   "5359242"   "5436574"   "5457644"   "5481206"   "5483478"   "5523963"   "5546018").PN. OR ("5761099").URPN.	US-PGPUB; USPAT; USOCR	OR	ON	2006/10/05 14:58
S20	361	708/700-714.ccls. and @ad<"20030911" and (LAB\$2 or (logic adj array adj block\$1) or table\$1 or LUT\$1)	US-PGPUB; USPAT; USOCR	OR	ON	2006/10/05 14:58
S21	321	S20 and carry and sum	US-PGPUB; USPAT; USOCR	OR	ON	2007/02/13 12:57
S22	16	S21 and (PLD or (programmable adj logic adj device))	US-PGPUB; USPAT; USOCR	OR	ON	2006/10/05 14:59

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S23	24	("20020089348"   "3473160"   "4546446"   "4871930"   "5122685"   "5128559"   "5333120"   "5371422"   "5483178"   "5497341"   "5570039"   "5689195"   "5754459"   "5825202"   "5874834"   "5892962"   "5999015"   "6069487"   "6215326"   "6343306"   "6407576"   "6538470"   "6556044").PN. OR ("7024446"). URPN.	US-PGPUB; USPAT; USOCR	OR	ON	2006/10/05 15:00
S24	65	708/708.ccls. and @ad<"20030911"	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/10/05 15:10
S25	1	((programmable adj logic adj device) or PLD) and S24 and (LUT\$1 or table\$1)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/10/05 15:09

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IEEE JNL IEEE Journal or Magazine  
IET JNL IET Journal or Magazine  
IEEE CNF IEEE Conference Proceeding  
IET CNF IET Conference Proceeding  
IEEE STD IEEE Standard

- ☐ 1. An FPGA-based, 12-channel TDC and digital signal processing module for the RatCAP scanner  
Junnarkar, S.S.; Purschke, M.; Pratte, J.-F.; Sang-June Park; O'Connor, P.; Fontaine, R.;  
[Nuclear Science Symposium Conference Record, 2005 IEEE](#)  
Volume 2, 23-29 Oct. 2005 Page(s):919 - 923  
Digital Object Identifier 10.1109/NSSMIC.2005.1596404  
[AbstractPlus](#) | Full Text: [PDF\(1139 KB\)](#) IEEE CNF  
[Rights and Permissions](#)
- ☐ 2. User configurable logic  
Fouk, P.W.;  
[Computing & Control Engineering Journal](#)  
Volume 3, Issue 5, Sept. 1992 Page(s):205 - 213  
[AbstractPlus](#) | Full Text: [PDF\(688 KB\)](#) IET JNL
- ☐ 3. Built-in self-test and fault diagnosis for lookup table FPGAs  
Shyue-Kung Lu; Jen-Sheng Shih; Cheng-Wen Wu;  
[Circuits and Systems, 2000. Proceedings. ISCAS 2000 Geneva. The 2000 IEEE International Symposium on](#)  
Volume 1, 28-31 May 2000 Page(s):80 - 83 vol.1  
Digital Object Identifier 10.1109/ISCAS.2000.857031  
[AbstractPlus](#) | Full Text: [PDF\(368 KB\)](#) IEEE CNF  
[Rights and Permissions](#)
- ☐ 4. A novel approach to testing LUT-based FPGAs  
Shyue-Kung Lu; Cheng-Wen Wu;  
[Circuits and Systems, 1999. ISCAS '99. Proceedings of the 1999 IEEE International Symposium on](#)  
Volume 1, 30 May-2 June 1999 Page(s):173 - 177 vol.1  
Digital Object Identifier 10.1109/ISCAS.1999.777831  
[AbstractPlus](#) | Full Text: [PDF\(416 KB\)](#) IEEE CNF  
[Rights and Permissions](#)
- ☐ 5. A silicon efficient FLEX 6000 programmable logic architecture  
Chiakang Sung; Cliff, R.; Huang, J.; Wang, B.; Khai Nguyen; Xiaobao Wang; Veenstra, K.; Pedersen, B.; Turner, J.;  
[Custom Integrated Circuits Conference, 1998.. Proceedings of the IEEE 1998](#)  
11-14 May 1998 Page(s):273 - 276  
Digital Object Identifier 10.1109/CICC.1998.694979  
[AbstractPlus](#) | Full Text: [PDF\(652 KB\)](#) IEEE CNF  
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6. A 3.3-V programmable logic device that addresses low power supply and interface trends

- Patel, R.; Wong, W.; Lam, J.; Lai, T.; White, T.; Cheung, S.;  
Custom Integrated Circuits Conference, 1997., Proceedings of the IEEE 1997  
5-8 May 1997 Page(s):539 - 542  
Digital Object Identifier 10.1109/CICC.1997.606684  
[AbstractPlus](#) | Full Text: [PDF\(380 KB\)](#) IEEE CNF  
[Rights and Permissions](#)
7. **A 90.7 MHz-2.5 million transistors CMOS CPLD with JTAG boundary scan and in-system programmability**  
Patel, R.; Myron Wong; Costello, J.; Reese, D.; Bocchino, V.; Chu, M.; Turner, J.;  
Custom Integrated Circuits Conference, 1995., Proceedings of the IEEE 1995  
1-4 May 1995 Page(s):507 - 510  
Digital Object Identifier 10.1109/CICC.1995.518234  
[AbstractPlus](#) | Full Text: [PDF\(372 KB\)](#) IEEE CNF  
[Rights and Permissions](#)
8. **A 5000-gate CMOS EPLD with multiple logic and interconnect arrays**  
Wong, S.C.; So, H.C.; Ou, J.H.; Costello, J.;  
Custom Integrated Circuits Conference, 1989., Proceedings of the IEEE 1989  
15-18 May 1989 Page(s):5.8/1 - 5.8/4  
Digital Object Identifier 10.1109/CICC.1989.56697  
[AbstractPlus](#) | Full Text: [PDF\(188 KB\)](#) IEEE CNF  
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9. **Control logic modelling scheme well suited to test problem**  
Crestani, D.; Eudeline, L.; Aguila, A.; Chardon, P.; Gentil, M.-H.; Durante, C.;  
Electronics Letters  
Volume 27, Issue 11, 23 May 1991 Page(s):991 - 993  
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# Inventor Information for 10/660903

Inventor Name	City	State/Country
LANGHAMMER, MARTIN	SALISBURY	UNITED KINGDOM

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## Inventor Name Search Result

Your Search was:

Last Name = LANGHAMMER

First Name = MARTIN

Application#	Patent#	Status	Date Filed	Title	Inventor Name
<a href="#">09218974</a>	<a href="#">6317771</a>	150	12/22/1998	METHOD AND APPARATUS FOR PERFORMING DIGITAL DIVISION	LANGHAMMER, MARTIN
<a href="#">09511206</a>	<a href="#">6400290</a>	150	02/23/2000	NORMALIZATION IMPLEMENTATION FOR A LOGMAP DECODER	LANGHAMMER, MARTIN
<a href="#">09826527</a>	<a href="#">6978287</a>	150	04/04/2001	DSP PROCESSOR ARCHITECTURE WITH WRITE DATAPATH WORD CONDITIONING AND ANALYSIS	LANGHAMMER, MARTIN
<a href="#">09924354</a>	<a href="#">6628140</a>	150	08/07/2001	PROGRAMMABLE LOGIC DEVICES WITH FUNCTION-SPECIFIC BLOCKS	LANGHAMMER, MARTIN
<a href="#">09952223</a>	<a href="#">6586966</a>	150	09/13/2001	DATA LATCH WITH LOW-POWER BYPASS MODE	LANGHAMMER, MARTIN
<a href="#">09955645</a>	<a href="#">6538470</a>	150	09/18/2001	DEVICES AND METHODS WITH PROGRAMMABLE LOGIC AND DIGITAL SIGNAL PROCESSING REGIONS	LANGHAMMER, MARTIN
<a href="#">09955647</a>	<a href="#">6556044</a>	150	09/18/2001	PROGRAMMABLE LOGIC DEVICE INCLUDING MULTIPLIERS AND CONFIGURATIONS THEREOF TO REDUCE RESOURCE UTILIZATION	LANGHAMMER, MARTIN
<a href="#">09955654</a>	<a href="#">6566906</a>	150	09/18/2001	SPECIALIZED PROGRAMMABLE LOGIC REGION WITH LOW-POWER MODE	LANGHAMMER, MARTIN
<a href="#">09969977</a>	Not Issued	161	10/02/2001	Programmable logic integrated circuit devices including dedicated hard-wired functional units and processor object components	LANGHAMMER, MARTIN
<a href="#">09975094</a>	Not Issued	120	10/10/2001	Method and apparatus for protecting designs in SRAM-based programmable logic devices	LANGHAMMER, MARTIN
<a href="#">10032597</a>	<a href="#">7035356</a>	150	10/25/2001	EFFICIENT METHOD FOR TRACEBACK DECODING OF TRELLIS (VITERBI) CODES	LANGHAMMER, MARTIN
<a href="#">10132873</a>	<a href="#">6781408</a>	150	04/24/2002	PROGRAMMABLE LOGIC DEVICE WITH ROUTING CHANNELS	LANGHAMMER, MARTIN
<a href="#">10145322</a>	<a href="#">7003544</a>	150	05/14/2002	METHOD AND APPARATUS FOR GENERATING A SQUARED VALUE FOR A SIGNED BINARY NUMBER	LANGHAMMER, MARTIN
<a href="#">10212487</a>	<a href="#">7173985</a>	150	08/05/2002	METHOD AND APPARATUS FOR IMPLEMENTING A VITERBI DECODER	LANGHAMMER, MARTIN
<a href="#">10277627</a>	<a href="#">6987401</a>	150	10/22/2002	COMPARE, SELECT, SORT, AND MEDIAN-FILTER APPARATUS IN PROGRAMMABLE LOGIC DEVICES AND ASSOCIATED METHODS	LANGHAMMER, MARTIN
<a href="#">10331707</a>	Not Issued	61	12/30/2002	Method and apparatus for implementing a multiple constraint length Viterbi decoder	LANGHAMMER, MARTIN
<a href="#">10354440</a>	<a href="#">6771094</a>	150	01/28/2003	DEVICES AND METHODS WITH PROGRAMMABLE LOGIC AND DIGITAL SIGNAL PROCESSING REGIONS	LANGHAMMER, MARTIN
<a href="#">10357749</a>	Not Issued	93	02/03/2003	METHODS AND APPARATUS FOR OPTIMIZING A PROCESSOR CORE ON A PROGRAMMABLE CHIP	LANGHAMMER, MARTIN
<a href="#">10377962</a>	<a href="#">6693455</a>	150	02/26/2003	PROGRAMMABLE LOGIC DEVICE INCLUDING MULTIPLIERS AND CONFIGURATIONS THEREOF TO REDUCE RESOURCE UTILIZATION	LANGHAMMER, MARTIN
<a href="#">10384905</a>	<a href="#">6714042</a>	150	03/06/2003	SPECIALIZED PROGRAMMABLE LOGIC REGION WITH LOW-POWER MODE	LANGHAMMER, MARTIN
<a href="#">10437426</a>	<a href="#">6958624</a>	150	05/12/2003	DATA LATCH WITH LOW-POWER BYPASS MODE	LANGHAMMER, MARTIN
<a href="#">10625093</a>	<a href="#">7024446</a>	150	07/22/2003	CIRCUITRY FOR ARITHMETICALLY ACCUMULATING A SUCCESSION OF ARITHMETIC VALUES	LANGHAMMER, MARTIN

<a href="#">10660903</a>	Not Issued	71	09/11/2003	Arrangement of 3-input LUT's to implement 4:2 compressors for multiple operand arithmetic	LANGHAMMER, MARTIN
<a href="#">10678201</a>	Not Issued	41	10/03/2003	Multi-functional digital signal processing circuitry	LANGHAMMER, MARTIN
<a href="#">10718968</a>	Not Issued	41	11/21/2003	Logic cell supporting addition of three binary words	LANGHAMMER, MARTIN
<a href="#">10742746</a>	<a href="#">7142010</a>	150	12/19/2003	PROGRAMMABLE LOGIC DEVICE INCLUDING MULTIPLIERS AND CONFIGURATIONS THEREOF TO REDUCE RESOURCE UTILIZATION	LANGHAMMER, MARTIN
<a href="#">10746448</a>	Not Issued	30	12/24/2003	Programmable logic device with specialized functional block	LANGHAMMER, MARTIN
<a href="#">10778930</a>	<a href="#">6937062</a>	150	02/12/2004	SPECIALIZED PROGRAMMABLE LOGIC REGION WITH LOW-POWER MODE	LANGHAMMER, MARTIN
<a href="#">10783789</a>	Not Issued	30	02/20/2004	Flexible accumulator in digital signal processing circuitry	LANGHAMMER, MARTIN
<a href="#">10783820</a>	Not Issued	30	02/20/2004	Multiplier-accumulator block mode splitting	LANGHAMMER, MARTIN
<a href="#">10783829</a>	Not Issued	30	02/20/2004	Saturation and rounding in multiply-accumulate blocks	LANGHAMMER, MARTIN
<a href="#">10807796</a>	Not Issued	30	03/23/2004	Digital signal processor	LANGHAMMER, MARTIN
<a href="#">10867456</a>	<a href="#">7084664</a>	150	06/14/2004	INTEGRATED CIRCUITS WITH REDUCED INTERCONNECT OVERHEAD	LANGHAMMER, MARTIN
<a href="#">10871868</a>	<a href="#">7119576</a>	150	06/18/2004	DEVICES AND METHODS WITH PROGRAMMABLE LOGIC AND DIGITAL SIGNAL PROCESSING REGIONS	LANGHAMMER, MARTIN
<a href="#">10874790</a>	<a href="#">7109753</a>	150	06/22/2004	PROGRAMMABLE LOGIC DEVICE WITH ROUTING CHANNELS	LANGHAMMER, MARTIN
<a href="#">10932210</a>	Not Issued	30	09/01/2004	Method and apparatus for implementing a look-ahead for low radix montgomery multiplication	LANGHAMMER, MARTIN
<a href="#">10938220</a>	Not Issued	30	09/10/2004	Method and apparatus for protecting designs in SRAM-based programmable logic devices and the like	LANGHAMMER, MARTIN
<a href="#">10986428</a>	Not Issued	30	11/10/2004	Mixed-mode multiplier using hard and soft logic circuitry	LANGHAMMER, MARTIN
<a href="#">11030801</a>	Not Issued	30	01/07/2005	Data compression using dummy codes	LANGHAMMER, MARTIN
<a href="#">11042019</a>	Not Issued	30	01/25/2005	FPGA configuration bitstream encryption using modified key	LANGHAMMER, MARTIN
<a href="#">11042032</a>	Not Issued	30	01/25/2005	Encryption key obfuscation and storage	LANGHAMMER, MARTIN
<a href="#">11042477</a>	Not Issued	30	01/25/2005	FPGA configuration bitstream protection using multiple keys	LANGHAMMER, MARTIN
<a href="#">11042937</a>	Not Issued	25	01/25/2005	One-time programmable memories for key storage	LANGHAMMER, MARTIN
<a href="#">11049072</a>	<a href="#">7109895</a>	150	02/01/2005	HIGH PERFORMANCE LEMPEL ZIV COMPRESSION ARCHITECTURE	LANGHAMMER, MARTIN
<a href="#">11138895</a>	Not Issued	160	05/25/2005	Specialized programmable logic region with low-power mode	LANGHAMMER, MARTIN
<a href="#">11145458</a>	Not Issued	30	06/02/2005	Method and apparatus for limiting use of IP	LANGHAMMER, MARTIN
<a href="#">11151743</a>	Not Issued	30	06/13/2005	Compare, select, sort, and median-filter apparatus in programmable logic devices and associated methods	LANGHAMMER, MARTIN
<a href="#">11155241</a>	Not Issued	30	06/17/2005	Programmable logic integrated circuit devices including dedicated processor components and hard-wired functional units	LANGHAMMER, MARTIN
<a href="#">11201945</a>	Not Issued	30	08/10/2005	DSP processor architecture with write Datapath word conditioning and analysis	LANGHAMMER, MARTIN
<a href="#">11208906</a>	Not Issued	30	08/22/2005	Programmable logic device with routing channels	LANGHAMMER, MARTIN

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